UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/045,043	01/15/2002	Chul-Min Kim	1349.1045	2926

21171 7590 12/16/2004

STAAS & HALSEY LLP
SUITE 700
1201 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER	
CHOW, CHARLES CHIANG	
ART UNIT	**PAPER NUMBER**
2685	

DATE MAILED: 12/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/045,043	KIM ET AL.	
	Examiner	Art Unit	
	Charles Chow	2685	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9-19* is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☒ Claim(s) *6-8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/16/03; 10/6/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Iwase et al. (US 5,710,999).

Regarding claim 1, Iwase et al. (Iwase) teaches a tuner block (Fig. 1, Fig. 18A, Fig. 19, abstract), a tuner which tunes a broadcasting signal (the tuner for demodulating different broadcast radio frequencies, col. 1, lines 18-32), an IF/demodulator circuit which demodulates the broadcasting signal tuned by the tuner (~~the IF demodulator, Fig. 18A, for providing demodulated IF output at terminal 507, and the~~ demodulated audio, video at terminal 519, 517, col. 12, line 66 to col. 13, line 37), a modulator which modulates an input video signal and an input audio signal into RF signal (the circuitry taking video in at 523, audio in at 528 and providing RF out signal at terminal 534, Fig. 18A, col. 13, line 58 to col. 14, line 6), a casing which accommodates the tuner 538 , the IF/demodulator circuit and the modulator (the housing, 550, 551, contains the tuner, demodulator 536, col. 14, line 22-58; the housing contains the tuner having PLL 510, mixer 504, and IF amplifier 506, the RF modulator converter 536 in Fig. 18A, and the demodulator 539 in Fig. 18B), a plurality of pins disposed consecutively on an outer side of the casing (terminals 519-528, Fig. 19), the plurality of pins to input and/or output signals (the terminals for video in/out 523/517, audio in/out 528/519) and a voltage to operate the tuner, the IF/demodulator circuit and the modulator (the voltage from power source terminal 579 or 556 for operating tuner PLL 510,

mixer 504 and IF amplifier 506, RF modulator converter 536 in Fig. 18A, and the demodulator 539 in Fig. 18B), wherein one of the plurality of pins is power supply pin through which an electrical power is supplied from an outside power supply, and the tuner and the modulator are connected commonly to the power supply pin inside of the casing (the single power source from either 103 or 107, is fed through tuner connector 114 and the demodulation connector to the tuner 104 and demodulator unit 108, inside the housing, col. 5, lines 31-39).

Regarding **claim 2**, Iwase teaches among the plurality of pins a first pin through a fifth pin are used by modulator (the terminal pins 523, 528 of the video-in, audio-in, Fig. 18A, Fig. 18B-19, are showing the obviously of using pins for RF modulator converter 536 in Fig. 18A), a sixth pin through an eleventh pin and a fourteenth pin are used by the tuner (the pin 508, data-in is used for tuner connected to 501-502), and twelfth pin, a thirteenth pin, and sixteenth pin are used by the IF/demodulator circuit (the pin 507, 522, IF-out, AGC-in, the audio/video out 517/519, Fig. 18A, Fig. 18B-19, are demodulating circuitry).

Regarding **claim 3**, Iwase teaches among the plurality of pins a fifteenth pin is a reserved pin which is not used (the terminal pins between 528 and 523 are not used as shown in Fig. 19).

Regarding **claim 4**, Iwase teaches the third pin is the power supply pin (the power supply terminal 556 could obviously be a third pin for supplying power to the apparatus, depending upon the designer's choice).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iwase in view of Levine (US 5,915,068).

Regarding **claim 5**, Iwase fails to teaches the among the plurality of pins a seventh pin is a clock input pin which inputs a clock signal for use in the modulator and the tuner. However, Levine teaches these features, the modulator 36 for receiving clock signal form clock 30 (Fig. 2) in order to synchronize modulator 36 for alphanumeric message display on television screen (abstract, col. 3, lines 42-56, col. 4, lines 20-47). Levine teaches the programmable VCR for the operator interactively programmable routing display by utilizing the television screen, to flexibly displaying the programming routine in the video recorder with less cost (col. 1, line 28-66). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify Iwase with Levine's clock signal for modulator 36, such that modulator could be synchronized to the clock signal for displaying of the video recorder programmable routing on the television screen.

Claims Objection

3. Claims 6-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art fails to teach the in second pin is channel selection pin for inputs a channel selection signal which selects an output channel of the modulator in **claim 6**; the eleventh pin is an AFT pin which outputs a reference voltage to the CPU to

enable an automatic fine tuning AFT, and the fourteenth pin is a TU-V pin which outputs another reference voltage used to determine local oscillation frequency in **claim 7**; Regarding objected **claim 8**, it is because of the dependency upon claim 7.

Allowable Subject Matter

4. The following is an examiner's statement of reasons for allowance:

Claims 9-19 are allowable over the prior art of record, the prior art fails to teach singly, particularly, or in combination, the subject matter, for the tuner which tunes to a broadcast signal, wherein an SIF output pin disposed adjacent to the audio output pin for output a sound subcarrier SIF, and a clock input pin distanced from the SIF output pin by at least six pin intervals, the clock input pin to input clock signal to the modulator and tuner [**in claim 9**]; a tuner having a second pin input a channel selection signal to select an output channel of the modulator, and a ninth pin input another clock signal used to communicate with a CPU, a tenth pin input a command transmitted from CPU, and eleventh pin outputs a reference voltage to the CPU to enable automatic fine tuning AFT, a fourteenth pin outputs another reference voltage to determine local oscillation of a frequency required by the selected channel [**in claim 16**]; an interfacing circuit for selectively using one of a first tuner block and a second tuner block, **a first switch connects** a first of the corresponding pins to a power supply to selectively use the first tuner or connects the first corresponding pin to an audio output to selectively use the second tuner block, **a second switch disconnects** a clock input signal, **a third switch** which connects the clock input to a third of the corresponding pins, **a fourth switch** connects the third corresponding pin to a sound sub-carrier SIF, **a fifth switch** disconnects an automatic fine tuning output AFT, **a sixth switch** connects a video output to a

fifth of the corresponding pins to selectively use the second tuner and disconnects the fifth corresponding pin from the video output to selectively use the first tuner block [**in claim 17**]; An interfacing circuit for selectively using one of the **first tuner block and a second tuner block, a first jumper** which completes a first of the **plurality of circuit paths** to connect a first of the corresponding pins to a power supply input to selectively use the first tuner block or to connect the first corresponding pin to an audio output to selectively use the second tuner block, **a second jumper** completes a third of the **plurality of circuit paths** to connect a clock input to a second of the corresponding pins to selectively use the second tuner block or completes a fourth of the plurality of circuit paths to clock input to a third of the corresponding pins to selectively use the first tuner block [**in claim 18**]. The dependent claims are also allowable due to their dependency upon the independent claims.

The closest patent to **Iwase (US 5,710,999)** teaches the tuner, for broadcast signal, having IF/demodulator, modulator, casing, and plurality of pin terminals disposed consecutively at intervals on an outer side of the casing, the input and or output signal pins, a voltage for operating the tuner, IF/demodulator, modulator, as shown claim 1 above. Iwase fails to teach an SIF output pin disposed adjacent to the audio output pin for output a sound subcarrier SIF, and a clock input pin distanced from the SIF output pin by at least six pin intervals, the clock input pin to input clock signal to the modulator and tuner; the clock input pin to input clock signal to the modulator and tuner; a tuner having a second pin input a channel selection signal to select an output channel of the modulator, and a ninth pin input another clock signal used to communicate with a CPU, a tenth pin input a command transmitted from CPU, and eleventh pin outputs a reference voltage to the CPU to enable automatic fine tuning AFT, a

fourteenth pin outputs another reference voltage to determine local oscillation of a frequency required by the selected channel; the first switch to sixth switches, the first and second jumpers.

Sasaki (US 2003/0063,225 A1) teaches the video apparatus tuner mounting board having **plurality of circuit paths** and pin wholes for mounting different tuners, tuners 10, 20, having **switches 7-1, 7-2, 8-1, 8-2,** for enabling signals for different tuners (abstract, Fig. 1-3, [0010-0012, 0022-0024, --27-0028]. Sasaki fails to teach an SIF output pin disposed adjacent to the audio output pin for output a sound subcarrier SIF, and a clock input pin distanced from the SIF output pin by at least six pin intervals, the clock input pin to input clock signal to the modulator and tuner; the clock input pin to input clock signal to the modulator and tuner; a tuner having a second pin input a channel selection signal to select an output channel of the modulator, and a ninth pin input another clock signal used to communicate with a CPU, a tenth pin input a command transmitted from CPU, and eleventh pin outputs a reference voltage to the CPU to enable automatic fine tuning AFT, a fourteenth pin outputs another reference voltage to determine local oscillation of a frequency required by the selected channel; the first switch to sixth switches, the first and second jumpers.

Kohn (US 4,509,210) teaches the television receiver with adaptable descrambler module (abstract, Fig. 1-2) having connector 40 with jumper in Fig. 2 for **signal connection jumpers** to adapt different descrambler module (col. 5, lines 9-53). Kohn fails to teach the above mentioned claimed features, for the jumpers, switches, for claims 9, 16-18.

Other prior arts in below has been considered, but they fail to teach the above claimed features.

Terada et al. (US 5,475,876 B1) teaches the tuner unit having electromagnetically isolated UHF and VHF section with no noise (abstract, Fig. 5) having modulator IC 10, tuner and demodulator with mode switch 101, audio/video input signals, clock, data, enable signals, If output signals. Terada et al. fail to teach the above mentioned claimed features for SIF output pin disposed adjacent to the audio output pin for output a sound subcarrier SIF, and a clock input pin distanced from the SIF output pin by at least six pin intervals, the clock input pin to input clock signal to the modulator and tuner; the clock input pin to input clock signal to the modulator and tuner; a tuner having a second pin input a channel selection signal to select an output channel of the modulator, and a ninth pin input another clock signal used to communicate with a CPU, a tenth pin input a command transmitted from CPU, and eleventh pin outputs a reference voltage to the CPU to enable automatic fine tuning AFT, a fourteenth pin outputs another reference voltage to determine local oscillation of a frequency required by the selected channel; the first switch to sixth switches, the first and second jumpers. Other patent, Takahama (US 4,569,084), Hall et al. (US 6,404,309 B1), Ohwaki et al. (US 5,913,173), Kim (US 6,483,554 B1), Kubo et al. (US 5,355,532), Nagai et al. (US 5,457,817), Kumanoto et al. (US 4,691,378), they failed to teach SIF output pin disposed adjacent to the audio output pin for output a sound subcarrier SIF, and a clock input pin distanced from the SIF output pin by at least six pin intervals, the clock input pin to input clock signal to the modulator and tuner; the clock input pin to input clock signal to the

modulator and tuner; a tuner having a second pin input a channel selection signal to select an output channel of the modulator, and a ninth pin input another clock signal used to communicate with a CPU, a tenth pin input a command transmitted from CPU, and eleventh pin outputs a reference voltage to the CPU to enable automatic fine tuning AFT, a fourteenth pin outputs another reference voltage to determine local oscillation of a frequency required by the selected channel; the first switch to sixth switches, the first and second jumpers.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles Chow whose telephone number is (703)-306-5615.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Urban, can be reached at (703)-305-4385.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to: (703) 872-9306 (for Technology Center 2600 only)

Hand-delivered responses should be brought to 220 South 20th Street, Crystal Plaza Two, Lobby, Room 1B03, Arlington, VA 22202 (Customer Window).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Charles Chow C.C.

November 22, 2004.

EDWARD F. URBAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600